Application for United States Letters Patent

for

UTILIZING SLOW ASIC LOGIC BIST TO PRESERVE TIMING INTEGRITY ACROSS TIMING DOMAINS

by

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BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention pertains to **b**uilt-**i**n **s**elf-**t**esting ("BIST") of **a**pplication **s**pecific **i**ntegrated **c**ircuit ("ASIC") devices, and, more particularly, to a dual mode BIST controller.

2. DESCRIPTION OF THE RELATED ART

The evolution of computer chips typically spawns ever more complex integrated circuits. Manufacturers continually seek to fabricate more and smaller integrated circuit components in smaller areas. The effort pushes the abilities of technology in a number of areas including design, fabrication, and testing. In particular, as integrated circuits become more complex, they become more difficult to test, as do the computer chips, or "devices," into which they are fabricated.

The difficulty in testing integrated circuit devices affects not only the manufacturer. Frequently, a chip vendor will contract with a manufacturer to make chips on specification for them to sell. Just as the manufacturer wants to test the devices to make sure they meet applicable quality standards, the vendors want to make sure the devices they purchase meet the standards they set. This common concern has led the industry to develop several conventional approaches to testing integrated circuit devices.

One approach to testing integrated circuits is "**b**uilt **i**n **s**elf-**t**esting," or "BIST." In BIST, in addition to "core" integrated circuits that provide the functionality of the device, the device includes integrated circuitry dedicated to testing. In this sense, the testing capability is "built-in" to the integrated circuit device. On receiving a predetermined signal, the BIST circuitry tests the core integrated circuitry and indicates whether it functions as designed. In this sense, the integrated circuit is self-testing in that it performs the test itself upon receipt of the externally generated test signal.

BIST comes in at least two variations. One is "memory" BIST, or "MBIST," and the other is "logic" BIST, or "LBIST." The MBIST tests the memory components of the device and the LBIST tests the logic on the device. An industry group called the **J**oint **T**est **A**ction **G**roup ("JTAG") developed an industry standard for interfacing with integrated circuit devices during tests. The JTAG standard is used with both variations of BIST. The integrated circuit device is manufactured with a JTAG "tap controller." The device is then tested in a live system or placed upon a chip tester. The live system or the chip tester generates a JTAG BIST signal input to the JTAG tap controller, which then begins the BIST. LBIST and MBIST can be used separately or in conjunction. The results of the BIST then tell the operator (if in a live system) or the vendor or manufacturer (if in a chip tester) whether and to what degree the device functions.

While BIST has many advantages and many uses, it also has some drawbacks. The logic and wiring with which the BIST are implemented take up valuable "real estate" on the die of the device. They also complicate the placement of device components and the routing of the connections between them. One reason for this complication is that the logic and circuitry implementing the BIST are distributed across the die. Another reason is that, during the design process, the LBIST and the MBIST are designed as separate "modules," or black boxes defined by their functions. Still another reason is that LBIST and MBIST operate in different time domains, and require separate clock signals. LBIST is further complicated by the fact that different parts of an ASIC typically operate at different frequencies, and signals from one domain into another can cause timing violations invalidating the LBIST results.

SUMMARY OF THE INVENTION

The invention, in its various aspects and embodiments, is a built-in self-test controller capable of performing a logic built-in self-test at a test frequency at least as slow as a slowest frequency of a plurality of timing domains to undergo the logic built-in self-test. A method for performing a built-in self-test on an integrated circuit device.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may be understood by reference to the following description taken in conjunction with the accompanying drawings, in which like reference numerals identify like elements, and in which: